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In re application of

MIRON ABRAMOVICI ET AL.

Serial No.: 09/994,299

: Group Art Unit: 2133

Filed: November 26, 2001

For: IDENTIFYING FAULTY PROGRAMMABLE INTERCONNECT  
RESOURCES OF FIELD PROGRAMMABLE GATE ARRAYS

TRANSMITTAL OF FORMAL DRAWINGS

Official Draftsperson  
Assistant Commissioner  
of Patents  
Washington, D.C. 20231

Sir:

Transmitted herewith are four (4) sheets of formal drawings to be submitted in  
lieu of the informal drawings previously filed in the above-identified application.

Respectfully submitted,

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Date \_\_\_\_\_

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graph LR
    10[FPGA UNDER TEST] <--> 12[CONTROLLER]
    12 <--> 14[MEMORY]
  
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Diagram illustrating a vehicle interior layout. The layout is divided into two main sections: a 'SELF-TESTING AREA' on the left and a 'WORKING AREA' on the right. A curved arrow labeled '10' points towards the right side of the diagram. The left side is labeled '16' and the right side is labeled '18'.

FIG. 3

The diagram illustrates a data path 19. It begins with a START input to a TPG block 20. The TPG block 20 has a DONE output. The data path 19 consists of several segments 26 separated by nodes 28. Two of these segments 26 contain blocks 30. Nodes 29 are also present in the path. An ORA block 22 is connected to the path and has a PASS/FAIL output. Arrows 24 indicate the direction of signal flow.

FIG. 4

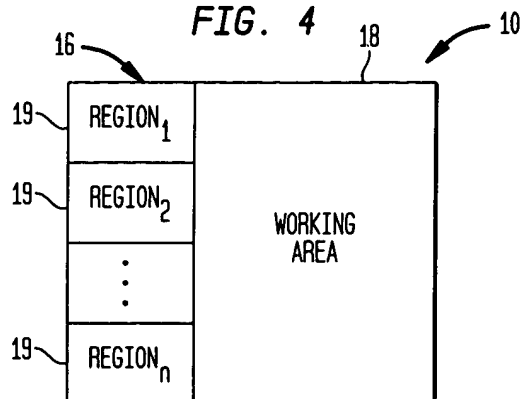


FIG. 5

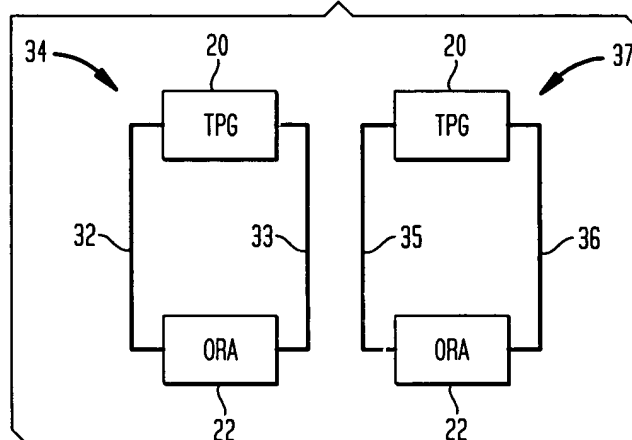


FIG. 6

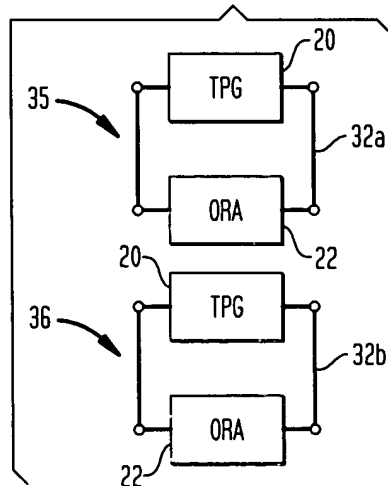


FIG. 7

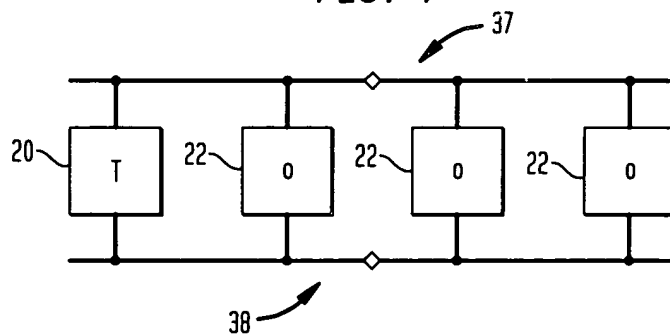


FIG. 8

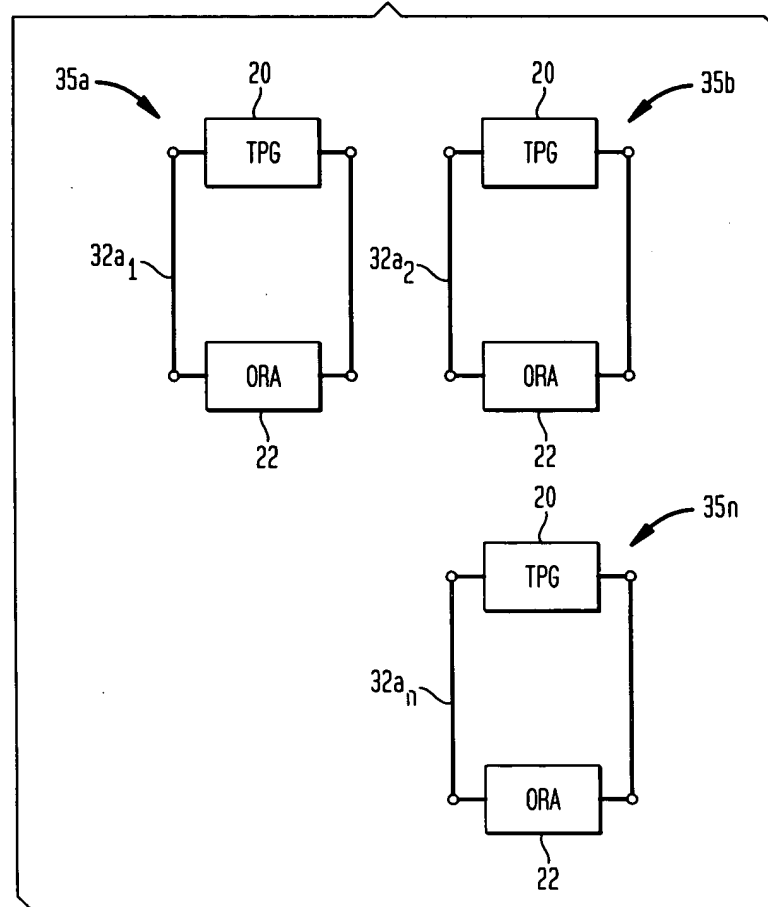


FIG. 9

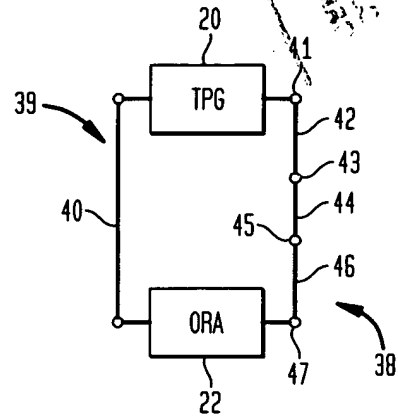


FIG. 10

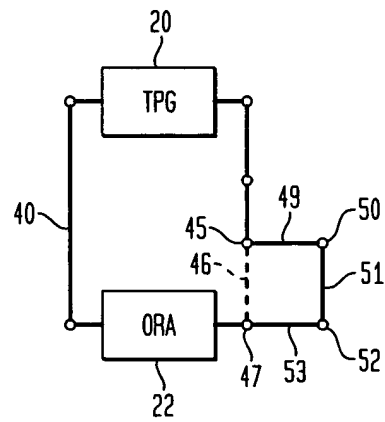


FIG. 11

